Curriculum Vitae

- **Name:** Abhijit Mallik
- **Specialization:** CMOS Devices, Microelectronics
- **Designation:** Professor
- **Affiliation & Contact Information:**

University of Calcutta

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- **Past Affiliations:**

  - Department of Electronics & Communication Engineering, Kalyani government Engineering College, Kalyani, India, from 1997 to 2007 (initially as Assistant Professor and re-designated as Associate Professor w.e.f. 1.1.2006).

  - Department of Electrical Engineering, Yale University, New Haven, USA, from 1994 to 1995 as a Postdoctoral Fellow. Worked on the process development and interface characterization of jet-vapor-deposited (JVD) silicon nitride as an alternative gate insulator for ultra-large-scale-integration (ULSI) applications.

  - Department of Electrical Engineering, Indian Institute of Technology, Bombay, India, as a Ph.D. student. Played a key role in standardizing an nMOS process and developing a radiation-hard chip going up to 1 Mrad(Si).

- **Educational Background:**
  - B. Sc. (Hons.) in Physics from the University of Calcutta (Presidency College) in 1986 (session 1982-1985).
  - M. Sc. in Electronic Science from the University of Calcutta in 1989 (Gold Medalist for securing 1st Class 1st position) (session 1985-1987).
  - Ph. D. in Electrical Engineering from the Indian Institute of Technology, Bombay, in 1994.
- **Research Interest:** Advanced CMOS Devices, Tunnel FET, Non-Volatile Memory Devices, Organic Electron Devices.
- **Membership of Scientific Bodies:** Senior Member: IEEE
- **Research Guidance:**
  - Postdoctoral: 02
  - Ph.D.: 14 (Awarded: 07, Submitted: 01, Pursuing: 06)
- **Patent**

  A. Mallik, "Tunnel Field-Effect Transistor (TFET) with Supersteep Subthreshold Swing," US Patent No. 9748368B2 dated Aug. 29, 2017, China Patent No. CN105378929B dated 22.06.2018, PCT Application No. PCT/IB2013/056828 dated 23.08.2013.
- **Books/Book Chapters:**

A. Book:

1. Y. Omura, **A. Mallik,** and N. Matsuo, "MOS Devices for Low-Voltage and Low-Energy Applications" Wiley-IEEE Press, Oct. 2016.

B. Book Chapters:

1. Y. Omura and **A. Mallik,** "Potential of Low-Voltage Low-Energy MOS Devices in Coming Sensor Network Era," in Advances in Microelectronics: Reviews, Book Series Vol. 01, IFSA Publishing.
2. E. Datta, A. Chattopadhyay, and **A. Mallik, "**Effect of Gate Dielectric Material on the Analog Performance of a Ge-Source Tunnel FET," in The Physics of Semiconductor Devices, Proc. of IWPSD-2017, Springer Proceedings in Physics (SPPHY), volume 215, January 2019.
3. S. Tewari, A. Biswas, and **A. Mallik, "**Investigations on the Logic Circuit Behavior of Hybrid CMOSFETs Comprising InGaAs nMOS and Ge pMOS

Devices with Barrier Layers" in Lecture Notes in Electrical Engineering, January 2018.

❖ **List of Research Projects:**

- Investigations of Organic Nano-Materials for Non-Volatile Memory Applications, D.S.T., Govt. of India, 2019-2022 (Ongoing), Principal Investigator.
- Device Design and Optimization of Complementary Tunnel FETs for Low Power Applications and Their Variability Study, SERB, D.S.T., Govt. of India, 2013-2016, Principal Investigator.
- Study of CMOS Devices and Circuits Utilising "Beyond Silicon" Channel Materials for ULSI Applications, CSIR, 2012-2015, Co-Investigator.
- Study and Modeling of Tunnel Field-Effect Transistor, D.S.T., Govt. of India, 2009-2013, Principal Investigator.
- Device Design and Modeling of Sub–45nm Schottky–Barrier MOSFETs, UGC, 2010-2013, Co-Investigator.
- Study and Modeling of Sub-Threshold Characteristics of Deep Sub-Micron Bulk and Thin-Film SOI CMOS Devices with and without Halo Implantation, D.S.T., Govt. of India, 2005-2008, Principal Investigator (in collaboration with Jadavpur University).
- Channel Engineering for Deep Sub-Micron MOSFETs, AICTE, 2000-2002, Principal Investigator.

❖ **List of Publications:**

A. <u>Journal</u>:

1. B. Das, M. Samanta, P. K. Sarkar, U. K. Gharai, **A. Mallik**, and K. K. Chattopadhyay, " Copper (II) Phthalocyanine (CuPc) Based Optoelectronic Memory Devices With Multilevel Resistive Switching for Neuromorphic Application," *Advanced Electronic Materials (Wiley)*, to appear, 2021.
2. M. Sil and **A. Mallik**, "On the Logic Performance of Bulk Junctionless FinFETs," *Analog Integrated Circuits and Signal Processing (Springer)*, (http://doi.org/10-1007/s10470-020-01782-y), 2021.
3. T. Ghosh, S. Mondal, R. Maiti, S. M. Nawaz, N. Ghosh, E. Dinda, A. Biswas, S. K. Maity, **A. Mallik**, and D. K. Maiti, "Complementary Amide-Based Donor-Acceptor with Unique Nano-Scale Aggregation, Fluorescence, and Bandgap Lowering Properties: a WORM Memory Device," *Nanotechnology (IOP)*, (https://doi.org/10.1088/1361-6528/abba5a), 2020.

4. S. M. Nawaz and **A. Mallik**, "Role of Quantum Capacitance on the Random Dopant Fluctuation Induced Threshold Voltage Variability in Junctionless InGaAs FinFETs," *Solid-State Electronics (Elsevier)* 171, 107862, 2020.
5. E. Datta, A. Chattopadhyay, **A. Mallik**, and Y. Omura, "Temperature Dependence of Analog Performance, Linearity, and Harmonic Distortion for a Ge-Source Tunnel FET," *IEEE Trans. Electron Devices*, vol. 67, no. 3, pp. 810-815, Mar. 2020.
6. E. Datta, A. Chattopadhyay, and **A. Mallik**, "Relative Study of Analog Performance, Linearity and Harmonic Distortion between Junctionless and Conventional SOI FinFETs at Elevated Temperatures," *Journal of Electronic Materials (Springer)*, 1-8, 2020.
7. M. Sil, S. Guin, S. M. Nawaz, and **A. Mallik**, "Performance of Ge p-channel junctionless FinFETs for logic applications," *Applied Physics A (Springer)* 125, 782, 2019.
8. Y. Jiang, S. Sato, Y. Omura, and **A. Mallik**, "Analysis of Miller Capacitance of Si Tunnel Field-Effect Transistors and Potential for Low-Voltage/Low-Energy Applications," *International Journal of Engineering Applications*, vol. 7, No. 3, pp. 88-96, 2019.
9. S. De, S. Tewari, S. De, A. Biswas, **A. Mallik**, "Improved digital performance of hybrid CMOS inverter with Si p-MOSFET and InGaAs n-MOSFET in the nanometer regime," *Microelectronic Engineering (Elsevier)*, vol. 211, pp. 18-25, 2019.
10. R. Basak, B. Maiti, and **A. Mallik**, "Effect of the Presence of Trap States in Oxides in Modeling Gate Leakage Current in Advanced MOSFET with Multi-Oxide Stack," *Superlattices and Microstructures (Elsevier)*, vol. 129, pp. 193-201, 2019.
11. Y. Omura, Y. Mori, S. Sato, and **A. Mallik**, "Revisiting the Role of Trap-Assisted-Tunneling Process on Current-Voltage Characteristics in Tunnel Field-Effect Transistors," *J. Appl. Phys.*, vol. **123**, pp. 161549-1-161549-6, Apr. 2018 (https://doi.org/10.1063/1.5010036).
12. S. Tewari, S. De, A. Biswas, and **A. Mallik**, "Impact of Sidewall Spacer on n-InGaAs Devices and Hybrid n-InGaAs/Si CMOS Amplifiers in Deca-Nanometer Regime," *Microsystem Technologies (Springer)*, 1-8, Dec. 2017 (https://doi.org/10.1007/s00542-017-3658-4).
13. D. K. Maiti, S. Debnath, S. M. Nawaz, B. Dey, E. Dinda, D. Roy, S. Ray, **A. Mallik**, and S. A. Hussain, "Composition-Dependent Nanoelectronics of Amido-Phenazines: Non-Volatile RRAM and WORM Memory Devices," *Scientific Reports (Nature Publishing Group)* 7, Article number: 13308, Oct. 2017.
14. S. De, S. Tewari, A. Biswas, and **A. Mallik**, "Impact of Channel Thickness and Spacer Length on Logic Performance of p-Ge/n-Si Hybrid CMOSFETs for ULSI Applications," *Superlattices and Microstructures (Elsevier)*, vol. 109, pp. 316-323, Sep. 2017.
15. Y. Mori, S. Sato, Y. Omura, A. Chattopadhyay, and **A. Mallik**, "On the Definition of Threshold Voltage for Tunnel FETs," *Superlattices and Microstructures (Elsevier)*, vol. 107, pp. 17-22, Jul. 2017.
16. S. Guin, M. Sil, and **A. Mallik**, "Comparison of Logic Performance of CMOS Circuits Implemented with Junctionless and Inversion-Mode FinFETs," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 953-959, Mar. 2017.

17. Y. Mori, S. Sato, Y. Omura, and **A. Mallik**, "Proposal of the Possible Method to Define the Threshold Voltage of Lateral Tunnel Field-Effect Transistors," *Technology Reports of Kansai University (Osaka, Japan*), vol. 59, pp. 75-81, Mar. 2017.

18. S. M. Nawaz and **A. Mallik**, "Effects of Device Scaling on the Performance of Junctionless FinFETs Due to Gate-Metal Work Function Variability and Random Dopant Fluctuations," *IEEE Electron Device Lett.,* vol. 37, no. 8, pp. 958-961, Aug. 2016.

19. S. Tewari, A. Biswas, and **A. Mallik**, "Impact of a Spacer Layer on the Analog Performance of Asymmetric InP/InGaAs nMOSFETs," *IEEE Trans. Electron Device,* vol. 63, no. 6, pp. 2313-2320, Jun. 2016.

20. S. M. Nawaz, S. Dutta, and **A. Mallik**, "Comparison of Gate-Metal Work Function Variability Between Ge and Si p-Channel FinFETs," *IEEE Trans. Electron Device,* vol. 62, no. 12, pp. 3951-3956, Dec. 2015.

21. S. M. Nawaz, S. Dutta, and **A. Mallik**, "A Comparison of Random Discrete Dopant Induced Variability between Ge and Si Junctionless p-FinFETs," *Appl. Phys. Lett.,* vol. 107, no. 3, pp. 033506-1-033506-4, Jul. 2015.

22. H. Lv, S. Sato, Y. Omura, and **A. Mallik**, "Analytically Modeling the Asymmetric Double Gate Tunnel FET," *ECS Trans.,* vol. 66, no. 5, pp. 193-200, 2015.

23. S. Sato, Y. Omura, and **A. Mallik**, "Compact Model for Nano-Wire Tunnel Field-Effect Transistor," *ECS Trans.,* vol. 66, no. 5, pp. 171-177, 2015.

24. A. Chattopadhyay, **A. Mallik**, and Y. Omura, "Device Optimization and Scaling Properties of a Gate-on-Germanium Source Tunnel Field-Effect Transistor," *Superlattices and Microstructures (Elsevier),* vol. 82, pp. 415-429, Jun. 2015.

25. S. Tewari, A. Biswas, and **A. Mallik**, "Performance of CMOS with Si p-MOS and Asymmetric InP/InGaAs n-MOS for Analog Circuit Applications," *IEEE Trans. Electron Device,* vol. 62, no. 5, pp. 1655-1658, May 2015.

26. R. Basak, B. Maiti, and **A. Mallik**, "Analytical Model of Gate Leakage Current Through Bilayer Oxide Stack in Advanced MOSFET," *Superlattices and Microstructures (Elsevier),* vol. 80, pp. 20-31, Apr. 2015.

27. S. Tewari, A. Biswas, and **A. Mallik**, "Investigation on High Performance CMOS with p-Ge and n-InGaAs MOSFETs for Logic Applications," *IEEE Trans. Nanotechnology,* vol. 14. no. 2, pp. 275-281, Mar. 2015.

28. **A. Mallik**, A. Chattopadhyay, and Y. Omura, "Gate-on-Germanium Source Tunnel Field-Effect Transistor Enabling Sub-0.5-V Operation," *Jpn. J. Appl. Phys.,* vol. 53, no. 10, pp. 1042011-1042017, Oct. 2014.

29. S. Guin, A. Chattopadhyay, A. Karmakar, and **A. Mallik**, "Impact of a Pocket Doping on the Device Performance of a Schottky Tunneling Field-Effect Transistor," *IEEE Trans. Electron Devices,* vol. 61, no. 7, pp. 2515-2522, Jul. 2014.

30. S. M. Nawaz, S. Dutta, A. Chattopadhyay, and **A. Mallik**, "Comparison of Random Dopant and Gate-Metal Workfunction Variability Between Junctionless and Conventional FinFETs," *IEEE Electron Device Lett.,* vol. 35, no. 6, pp. 663-665, Jun. 2014.

31. S. Tewari, P. K. Saha, A. Biswas, and **A. Mallik**, "Effects of Barrier Layer of Nanoscale InGaAs-Channel MOSFETs on Analog Circuit Performance," *An International Journal of Jaipur National University (INROADS) (Special Issue),* vol. 3, no. 1, pp. 168-172, Jan.-Jun. 2014.

32. S. Tewari, A. Biswas, and **A. Mallik**, "High Performance Logic Gates Built with Hybrid p-Ge/ n-InGaAs CMOS Inverters at Channel Length of 45 nm," *An International Journal of Jaipur National University (INROADS) (Special Issue),* vol. 3, no. 1, pp. 357-362, Jan-June, 2014.

33. **A. Mallik**, "Tunnel FETs for Mixed-Signal System-On-Chip Applications," *ECS Trans.*, vol. 53, issue 5, pp. 93-104, May 2013.

34. S. Tewari, A. Biswas, and **A. Mallik**, "Impact of Different Barrier Layers and In-Content of the Channel on the Analog Performance of InGaAs MOSFETs," *IEEE Trans. Electron Devices,* vol. 60, no. 5, pp. 1584-1589, May 2013.

35. **A. Mallik**, A. Chattopadhyay, S. Guin, and A. Karmakar, "Impact of a Spacer-Drain Overlap on the Characteristics of a Silicon Tunnel Field-Effect Transistor Based on Vertical Tunneling," *IEEE Trans. Electron Devices,* vol. 60, no. 3, pp. 935-943, Mar. 2013.

36. S. Tewari, A. Biswas, and **A. Mallik**, "Effects of a Barrier Layer in InGaAs Channel MOSFETs for Analog/Mixed Signal System-on-Chip Applications," *International Journal of Electrical and Electronics Engineering,* vol. 2, pp. 41-44, 2013.

37. **A. Mallik** and A. Chattopadhyay, "Observation of Current Enhancement Due to Drain-Induced Drain Tunneling in Tunnel Field-Effect Transistors," *Jpn. J. Appl. Phys.,* vol. 51, no. 8, pp. 0843011-0843014, Aug. 2012.

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40. **A. Mallik** and A. Chattopadhyay, "The Impact of Fringing Field on the Device Performance of a P-Channel Tunnel Field-Effect Transistor with a High-κ Gate Dielectric," *IEEE Trans. Electron Devices,* vol. 59, no. 2, pp. 277-282, Feb. 2012.

41. **A. Mallik** and A. Chattopadhyay, "Drain-Dependence of Tunnel Field-Effect Transistor Characteristics: The Role of the Channel," *IEEE Trans. Electron Devices,* vol. 58, no. 12, pp. 4250-4257, Dec. 2011.

42. S. Chakraborty, **A. Mallik,** and C. K. Sarkar, "Subthreshold Performance of Pocket-Implanted Silicon-On-Insulator CMOS Devices and Circuits for Ultra-Low-Power Analogue/Mixed-Signal Applications," *IET Circuits Devices Syst.*, vol. 5, no. 4, pp. 343–350, July 2011.

43. A. Chattopadhyay and **A. Mallik,** "Impact of a Spacer Dielectric and a Gate Overlap/Underlap on the Device Performance of a Tunnel Field-Effect Transistor," *IEEE Trans. Electron Devices,* vol. 58, no. 3, pp. 677-683, Mar. 2011.

44. P. Sarkar, **A. Mallik,** and C. K. Sarkar, "Study on the Performance of Sub 100nm LACLATI MOSFETs for Digital Applications," *Microelectronics Reliability (Elsevier),* vol. 49, no. 4, pp. 392-396, Apr. 2009.

45. P. Sarkar, **A. Mallik,** and C. K. Sarkar, "Single Halo SDODEL n- MOSFET: An Alternative Low Cost Pseudo-SOI with Better Analog Performance," *Semiconductor Science and Technology*, vol. 24, no.3, 035001 (6pp), Mar. 2009.

46. S. Chakraborty, **A. Mallik,** and C. K. Sarkar, "Subthreshold Performance of Dual Material Gate CMOS Devices and Circuits for Ultralow Power Analog/Mixed-Signal Applications", *IEEE Trans. Electron Devices*, vol. 55, no. 3, pp. 827-832, Mar 2008.

47. S. Baishya, **A. Mallik,** and C. K. Sarkar, "A Threshold Voltage Model for Short-Channel MOSFETs Taking into Account the Varying Depth of Channel Depletion Layers Around the Source and Drain," *Microelectronics Reliability (Elsevier),* vol. 48, no. 1, pp. 17-22, Jan. 2008.

48. S. Baishya, **A. Mallik,** and C. K. Sarkar, "A Pseudo Two-Dimensional Subthreshold Surface Potential Model for Dual-Material Gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2520-2525, Sep. 2007.

49. S. Baishya, **A. Mallik,** and C. K. Sarkar, "A Surface Potential Based Subthreshold Drain Current Model for Short-Channel MOS Transistors," *Semiconductor Science and Technology*, vol. 22, no.9, pp. 1066-1069, Sep. 2007.

50. P. Sarkar, **A. Mallik,** and C. K. Sarkar, "Performance Comparison of Channel Engineered Deep Sub-Micrometer Pseudo SOI n-MOSFETs," *Microelectronics Reliability (Elsevier),* vol. 47, no. 6, pp. 953-958, Jun. 2007.

51. S. Baishya, **A. Mallik,** and C. K. Sarkar, "Subthreshold Surface Potential and Drain Current Models for Short-Channel Pocket-Implanted MOSFETs," *Microelectronic Engineering (Elsevier),* vol. 84, no. 4, pp. 653-662, Apr. 2007.

52. S. Chakraborty, **A. Mallik,** C. K. Sarkar, and V. R. Rao, "Impact of Halo Doping on the Subthreshold Performance of Deep-Submicrometer CMOS Devices and Circuits for Ultralow Power Analog/Mixed-Signal Applications," *IEEE Trans. Electron Devices*, vol. 54, no. 2, pp. 241-248, Feb. 2007.

53. S. Baishya, S. Chakraborty, **A. Mallik,** and C. K. Sarkar, "A Subthreshold Surface Potential and Drain Current Model for Lateral Asymmetric Channel (LAC) MOSFET," *IETE Journal of Research (Special issue on Nanoelectronic Devices and Technology),* vol. 52, no. 5, pp. 379-390, Sep.-Oct. 2006.

54. S. Baishya, **A. Mallik,** and C. K. Sarkar, "A Subthreshold Surface Potential Model for Short Channel MOSFET Taking into Account the Varying Depth of Channel Depletion Layer Due to Source and Drain Junctions," *IEEE Trans. Electron Devices,* vol. 53, no. 3, pp. 507-514, Mar. 2006.

55. **A. Mallik,** X. W. Wang, T. P. Ma, G. J. Cui, T. Tamagawa, B. L. Halpern, and J. J. Schmitt, "Interface Traps in Jet-Vapor-Deposited Silicon Nitride-Silicon Capacitors," *J. Appl. Phys.,* vol. 79, no. 11, pp. 8507-8511, Jun. 1996.

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57. **A. Mallik,** J. Vasi, and A. N. Chandorkar, "Electron Trapping During Irradiation in Reoxidized Nitrided Oxide," *IEEE Trans. Nucl. Sci.,* vol. 40, no. 6, pp. 1380-1387, Dec. 1993.

58. **A. Mallik**, J. Vasi, and A. N. Chandorkar, "A Study of Radiation Effects on Reoxidized Nitrided Oxide MOSFETs, Including Effects on Mobility," *Solid-State Electron. (Elsevier),* vol. 36, no. 9, pp. 1359-1361, Sep. 1993.

59. **A. Mallik,** J. Vasi, and A. N. Chandorkar, "The Nature of the Hole Traps in Reoxidized Nitrided Oxide Gate Dielectrics," *J. Appl. Phys.,* vol. 74, no. 4, pp. 2665-2668, Aug. 1993.

60. A. Phanse, D. Sharma, **A. Mallik,** and J. Vasi, "Carrier Mobility Degradation in Metal-Oxide-semiconductor Field-Effect Transistors Due to Oxide Charge," *J. Appl. Phys.,* vol. 74, no. 1, pp. 757-759, Jul. 1993.

B. <u>Conferences</u>:

1. M. Sil and **A. Mallik**, "Comparative Performance of SRAM Cells Built with Inversion-Mode and Junctionless FinFETs," *XXth International Workshop on Physics of Semiconductor Devices: IWPSD 2019, Dec. 17-20, 2019, Kolkata, India (2019).*

2. E. Datta, A. Chattopadhyay, and **A. Mallik**, "Effects of Channel Doping Concentration on the Analog Performance of an InGaAs MOSFET," *XXth International Workshop on Physics of Semiconductor Devices: IWPSD 2019, Dec. 17-20, 2019, Kolkata, India (2019).*

3. B. Das, P. Sarkar, N. S. Das, **A. Mallik**, and K. K. Chattopadhyay, "Impact of Temperature on the Resistive Switching Behavior of PMMA Embedded $MoSe_2$-Based flexible RRAM Devices," *XXth International Workshop on Physics of Semiconductor Devices: IWPSD 2019, Dec. 17-20, 2019, Kolkata, India (2019).*

4. B. Das, P. Sarkar, P. Roy, **A. Mallik**, and K. K. Chattopadhyay, "Forming-Free Nonvolatile

Resistive Switching Memory Devices Based on PMMA Films with Embedded $MoSe_2$ Nanoflowers," *2nd International Conference on Nanoscience and Nanotechnology (ICNAN), 29th Nov- 1st Dec 2019, Vellore Institute of Technology, Vellore, India (2019).*

5. B. Das, P. Sarkar, N. S. Das, **A. Mallik**, and K. K. Chattopadhyay, "Topological Insulator Bi_2Se_3 Embedded in PMMA Hybrid Structures for Multifunctional Application: Photoresponsive and memory devices," *International Conference on Synthesis, Charecterization and Application of Nanomaterials (SCAN) 2019, Nov. 01-02, 2019, IIEST IIEST, Shibpur, India (2019).*

6. (invited) **A. Mallik,** "Future of Tunnel FET for Low-Power High-Frequency Applications," in *IEEE IMFEDK, June 21-22, 2018, Kyoto, Japan (2018).*

7. Y. Jiang, S. Sato, Y. Omura, and **A. Mallik,** "Aspects and Reduction of Miller Capacitance of Lateral Tunnel FETs," in *IEEE IMFEDK, June 21-22, 2018, Kyoto, Japan (2018).*

8. Y. Mori, S. Sato, Y. Omura, and **A. Mallik**, "Physical Mechanisms of Short-Channel Effects of Lateral Double-Gate Tunnel FET," in *IEEE IMFEDK, June 29-30, 2017, Kyoto, Japan (2017).*

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10. S. Tewari, S. De, A. Biswas, and **A. Mallik,** "Investigations on Logic Performance of p-Ge/n-Si Hybrid CMOSFETs for Digital Applications," *2nd International Conference on Nano-electronics, Circuits & Communication Systems (NCCS-2016), Dec. 25-26, 2016, Ranchi, India (2016).*

11. Y. Mori, S. Sato, Y. Omura, and **A. Mallik**, "A Possible Threshold Voltage Definition of Lateral Tunnel FET," in *IEEE Silicon Nanoelectronics Workshop (SNW), June 12-13, 2016, Honolulu, USA, pp. 188-189 (2016).*

12. S. M. Nawaz and **A. Mallik**, "Random Discrete Dopant Induced Threshold Voltage Variability in $In_xGa_{1-x}As$ Channel Junctionless FinFETs," in *18th International Workshop on Physics of Semiconductor Devices (IWPSD), Dec. 7-10, 2015, IISc, Bengalore, India* (2015).

13. S. Tewari, P. K. Saha, A. Biswas, and **A. Mallik,** "Investigations on the Logic Performance of Hybrid CMOSFETs Comprising p-Ge/ n-InGaAs MOSFETs with Barrier Layers," in *International Conference on Microelectronics, Computing & Communication Systems (MCCS-2015), Nov. 14-15, 2015, Ranchi, India (2015).*

14. H. Lv, S. Sato, Y. Omura, and **A. Mallik**, "Two-Dimensional Model for Asymmetric Double-Gate Tunnel FET Considering the Source-Channel Junction Depletion Region," in *IEEE IMFEDK, June 4-5, 2015, Kyoto, Japan (2015).*

15. S. Tewari, A. Biswas, and **A. Mallik,** "Effects of Channel Barrier Layer on The Analog Performance of p-Ge/ n-InGaAs CMOS devices," in *International Conference on Emerging Technology Trends in Electronics, Communication & Networking (ET2ECN - 2014), Dec. 26 - 27, 2014, pp. 56-59.*

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17. S. Tewari, P. K. Saha, A. Biswas, and **A. Mallik**, "Effects of Barrier Layer of Nanoscale InGaAs-Channel MOSFETs on Analog Circuit Performance," in *1st International Conference on Innovative Advancements in Engineering and Technology (IAET-2014) March 7-8, 2014, Jaipur, India.*

18. S. Tewari, A. Biswas, and **A. Mallik**, "High Performance Logic Gates Built with Hybrid p-Ge/ n-InGaAs CMOS Inverters at Channel Length of 45 nm," in *1st International Conference on Innovative Advancements in Engineering and Technology (IAET-2014) March 7-8, 2014, Jaipur, India.*

19. S. De, S. Tewari, A. Biswas, and **A. Mallik**, "Studies on the Analog Performance of InGaAs-Channel Junctionless Transistors," in *International Conference on Innovation in Electronics and Communication Engineering (ICIECE), August 9-10, 2013, Hyderabad, India, pp. 676-680 (2013).* **(Best Paper Award).**

20. S. Tewari, A. Biswas, and **A. Mallik**, "Studies on Digital Performance of CMOS Comprising Ge p-MOSFET and InGaAs n-MOSFET with Different In Contents," in *International Conference on Innovation in Electronics and Communication Engineering (ICIECE), August 9-10, 2013, Hyderabad, India, pp. 667-671 (2013).* (**Best Paper Award**).

21. S. Guin, A. Chattopadhyay, A. Karmakar, and **A. Mallik**, "Influence of a Pocket Doping in a Schottky Tunneling FET," in *IEEE IMFEDK, June 5-6, 2013, Osaka, Japan (2013).*

22. (Invited) **A. Mallik**, "Tunnel FETs for Mixed-Signal System-On-Chip Applications," in *223rd ECS Meeting, May 12-16, 2013, Toronto, Canada (2013).*

23. S. Tewari, A. Biswas, and **A. Mallik**, "Impact of Indium Contents on the Analog Circuit Performance of InGaAs channel MOSFETs," in *International Conference on Electrical, Electronics and Computer Science (ICEECS), March 24, 2013 Chandigarh, India (ISBN : 978-93-81693-88-16), pp. 178-181 (2013).*

24. **A. Mallik** and A. Chattopadhyay, "Spacer-Drain Overlap Dependence of Subthreshold Characteristics for Tunnel Field-Effect Transistor Based on Vertical Tunneling," in *IEEE International Conference on Emerging Electronics (ICEE), Dec. 15-17, 2012, Mumbai, India (2012).*

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40. S. Chakraborty, S. Baishya, **A. Mallik,** and C. K. Sarkar, "Performance Evaluation of Analog Circuits with Deep Submicrometer MOSFETs in the Subthreshold Regime of Operations," in *IEEE International Conference on Industrial and Information Systems (ICIIS), Aug. 8-11, 2006, Peradeniya, Sri Lanka*, pp. 99-102 (2006).

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45. P. Sarkar, **A. Mallik,** C. K. Sarkar, and V. R. Rao, "Performance of Channel Engineered SDODEL MOSFET for Mixed Signal Applications*,"* in *IEEE Conference on Electron Devices and Solid-State Circuits, Dec. 19-21, 2005, Hong Kong*, pp. 687-690 (2005).

46. A. Pal, R. Saha, S. Saha, S. Kundu, and **A. Mallik,** "Study of Capacitor-Less 1T-DRAM Cell Using Partially Depleted SOI MOSFET," in *International Conference on Communications, Devices & Intelligent Systems, Jan.8-10, 2004, Kolkata, India,* Jadavpur University, Kolkata, pp. 408-411.

47. **A. Mallik,** P. Ghosh, P. Das, T. Paul, and R. Das, "Inversion Layer Carrier Mobility in MOSFETs with Oxynitride Gate Dielectrics," in *Conference on Intelligent Computing and VLSI, Feb. 16-17, 2001, Kalyani, India,* Allied Publishers Limited, New Delhi, pp. 201-205.
48. **A. Mallik,** X. W. Wang, T. P. Ma, G. J. Cui, T. Tamagawa, B. L. Halpern, and J. J. Schmitt, "Properties of Interface Traps in JVD Silicon Nitride MNS Capacitors," in *IEEE Semiconductor Interface Specialist Conference (SISC), Dec. 7-9, 1995, Charleston, USA.*
49. **A. Mallik,** J. Vasi, and A. N. Chandorkar, "Hole Traps in Reoxidized Nitrided Oxide Gate Dielectrics," in *7th International Workshop on Physics of Semiconductor Devices (IWPSD), Dec. 14-18, 1993, New Delhi, India,* Narosa Publishing House, New Delhi, pp. 354-357.
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53. **A. Mallik,** J. Vasi, and A. N. Chandorkar, "Process Dependence of Radiation Hardness of Reoxidized Nitrided Oxide," in *Seminar on Physics and Technology of Semiconductor Devices, Sept. 21-22, 1992, Pilani, India*.
54. R. M. Patrikar, **A. Mallik,** L. Vijayraghavan, R. Lal, and A. N. Chandorkar, "Flatband Voltage Shift Due to Irradiation on Pyrogenic Oxide," in *6th International Workshop on Physics of Semiconductor Devices (IWPSD), Dec. 2-6, 1991, New Delhi, India*, Tata McGraw Hill Publishing Co. Ltd., New Delhi, pp. 510-512.

- **Foreign Visits:**
  - Yale University, New Haven, Connecticut, USA, 1994-95 (Postdoctoral Fellow).
  - Toronto, Canada, May 2013 (to deliver invited talk at the 223rd ECS meeting).
  - Osaka Japan, June 2013 (to present a paper in *IEEE IMFEDK-2013* and to deliver a talk at the Kansai University).
  - Kyoto, Japan, June 2018 (to deliver invited talk in *IEEE IMFEDK-2013).*
- **List of Invited Talk/Lectures**
  - National Conference on Recent Developments in Nanoscience & Nanotechnology (NCRDNN 2019)" Jan. 29-31, 2019.

- 3rd international conference "2019 Devices for Integrated Circuit (DevIC)", Kalyani Government Engineering College, March 23-24, 2019
- IEEE IMFEDK, Kyoto, Japan, Jun. 2018.
- UGC-HRDC Special Winter School, C.U., Mar. 2018.
- UGC-HRDC Winter School, C.U., Feb. 2017.
- STTP course on "Emerging devices and VLSI physical design" National Institute of Technology, Silchar, Oct. 2016.
- Workshop on "Nano-materials and Devices for Biomedical Applications," CRNN, Calcutta University, Oct. 2016.
- Faculty Development Program on "Modern Trends in Communication & Circuit Design, 2016 (MTCCD, 2KH)," Narula Institute of Technology, Kolkata, October, 2016.
- Refresher course on "Nanodevices and Low-Power VLSI Design", Jadavpur University, December 2013.
- Kansai University, Osaka, Japan, June 2013.
- 223rd ECS Meeting, Toronto, Canada, May 2013.
- UGC summer school, Department of Radio Physics and Electronics, University of Calcutta, May 2012.
- Visvesvaraya National Institute of Technology, Nagpur, September 2010.
- MHRD/AICTE sponsored summer school on "Nanotechnology for Electronic and Photonic Applications" at the Kolkata Campus of IIT-Kharagpur, July, 2009.
- UGC summer school on "NanoDev-09" Department of Radio Physics and Electronics, University of Calcutta, June, 2009.
- MHRD/AICTE summer school on "Nanoelectronics: Science, Nanotechnology, Engineering & Applications" at the Kolkata Campus of IIT-Kharagpur, June, 2008.
- UGC summer school on "Semiconductor Nanoelectronics- 2008" Department of Radio Physics and Electronics, Calcutta University, June, 2008.